93/B IFW

Docket No.: 071971-0643

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Shunsaku MURAOKA, et al.	:	Confirmation Number: 5602
Application No.: 10/584,617	:	Group Art Unit: 2824
	:	Allowed: August 7, 2008
Filed: June 26, 2006	:	Examiner: NGUYEN, NAM THANH

For: MEMORY DEVICE, MEMORY CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT HAVING VARIABLE RESISTANCE

LETTER UNDER 37 CFR 1.312

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

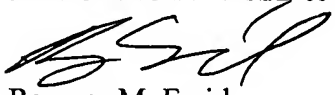
Sir:

The Notice of Allowance/Allowability (NOA) mailed on August 7, 2008 is acknowledged and appreciated. In the NOA, on page 2, second line from bottom – page 3, line 3 under the "Reasons for Allowance" section, the Examiner states that the prior art of record fail to teach "a second variable resistor connected between the third terminal and a second terminal having a resistance which changes in a direction opposite to a direction of change of the first variable resistor in accordance with a polarity of a pulse voltage between the third terminal and the second terminal as recited in the independent claims 1 **and 39**" (emphasis added). However, it should be noted that the claim language referenced by the Examiner is not the precise language expressly contained in claim 39.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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